IN THE CLAIMS

1. - 40. (Previously Canceled)

41. (Amended) A circuit on a single substrate, comprising:

a logic device, wherein the logic device further includes a transistor with a [dielectric layer] gate dielectric having a first thickness including a top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a [dielectric layer] gate dielectric having a second thickness greater than the [dielectric layer] gate dielectric of the first thickness but less than 12 nanometers, wherein the [dielectric layer] gate dielectric of the second thickness is formed entirely of silicon dioxide (SiO2).

42. (Amended) The circuit of claim 41, wherein the [dielectric layer] gate dielectric having a first thickness includes a [dielectric layer] gate dielectric of less than 7 nanometers, wherein the [dielectric layer] gate dielectric has a bottom layer of silicon dioxide (SiO2), and wherein the top layer is silicon nitride (Si3N4).

43. (Amended) The circuit of claim 41, wherein the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the [dielectric layer] gate dielectric having a first thickness exhibits a strong resistance to boron penetration at high temperatures.

44. (Amended) The circuit of claim 43, wherein the top layer of the [dielectric layer] gate dielectric having a first thickness exhibits a strong resistance to boron penetration at temperatures above approximately 300 degrees Celsius.

45. (Amended) The circuit of claim 41, wherein the [dielectric layer] gate dielectric of a first thickness having a top layer which exhibits a high resistance to oxidation at high temperatures

includes a top layer of silicon nitride (Si3N4) which comprises approximately a third of the first thickness of the [dielectric layer] gate dielectric.

46. (Amended) The circuit of claim 45, wherein the top layer of the [dielectric layer] gate dielectric of the first thickness has a thickness of less than 2 nanometers.

47. (Amended) A system on a chip, comprising:

a logic device, wherein the logic device further includes a transistor with a [dielectric layer] gate dielectric having a first thickness of less than 7 nanometers including a top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a [diclectric layer] gate dielectric having a second thickness greater than the [dielectric layer] gate dielectric of the first thickness but less than 12 nanometers.

48. (Amended) The system of claim 47, wherein the [dielectric layer] gate dielectric having a first thickness includes a dielectric layer having a bottom layer of silicon dioxide (SiO2), and wherein the top layer is silicon nitride (Si3N4).

49. (Amended) The system of claim 47, wherein the logic device transistor and the memory device transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the [dielectric layer] gate dielectric having a first thickness exhibits a strong resistance to [illegible] at high temperatures.

50. (Amended) The system of claim 49, wherein the top layer of the [dielectric layer] gate diclectric having a first thickness exhibits a strong resistance to boron penetration at temperatures above approximately 300 degrees Celsius.

51. (Amended) The system of claim 49, wherein the top layer of the [dielectric layer] gate dielectric having a first thickness exhibits a strong resistance to boron penetration at temperatures above approximately 800 degrees Celsius.

52. (Amended) The system of claim 47, wherein the [dielectric layer] gate dielectric of a first thickness having a top layer which exhibits a high resistance to oxidation at high temperatures includes a top layer of silicon nitride (Si3N4) which comprises approximately a third of the first thickness of the [dielectric layer] gate dielectric .

53. (Amended) The circuit of claim 52, wherein the top layer of the [dielectric layer] gate dielectric of the first thickness has a thickness of less than 2 nanometers.

54. (Amended) The system of claim 52, wherein the [dielectric layer] gate dielectric of the second thickness is formed entirely of silicon dioxide (SiO2).

55. (Amended) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a [dielectric layer] first gate dielectric of a first thickness including:

a first dielectric layer of a first thickness less than 5 nanometers;

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second [dielectric layer] gate dielectric having a second thickness greater than the [dielectric layer] first gate dielectric of the first thickness.

56. (Previously Added) The circuit of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

57. (Previously Added) The circuit of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4).

58. (Amended) The circuit of claim 55, wherein the second [dielectric layer] gate dielectric of a second thickness includes a [dielectric layer] gate dielectric formed entirely of silicon dioxide (SiO2).

59. (Amended) The circuit of claim 55, wherein the second [dielectric layer] gate dielectric of a second thickness includes a [dielectric layer] gate dielectric having a thickness of less than 12 nanometers.

60. (Amended) The circuit of claim 55, wherein the top layer includes a top layer of silicon nitride (Si3N4) which comprises approximately a third of the first thickness of the first [dielectric layer] gate dielectric .

61. (Previously Added) The circuit of claim 55, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

62. (Amended) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a [dielectric layer] first gate dielectric of a first thickness including:

a first dielectric layer of a first thickness less than 5 nanometers;

a top layer which exhibits a high resistance to boron penetration at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second [dielectric layer] gate dielectric having a second thickness greater than the [dielectric layer] first gate dielectric of the first thickness.

63. (Previously Added) The circuit of claim 62, wherein the [illegible] layer together have a thickness of less than 7 nanometers (nm).

64. (Amended) The circuit of claim 62, wherein the first dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4).

65. (Amended) The circuit of claim 62, wherein the second [dielectric layer] gate dielectric of a second thickness includes a [dielectric layer] gate dielectric formed entirely of silicon dioxide (SiO2).

66. (Amended) The circuit of claim 62, wherein the second [dielectric layer] gate dielectric of a second thickness includes a [dielectric layer] gate dielectric having a thickness of less than 12 nanometers.

67. (Previously Added) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride (Si3N4) top layer which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

68. (Previously Added) The circuit of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

69. (Previously Added) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO2).

70. (Previously Added) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

71. (Previously Added) The circuit of claim 67, wherein the silicon nitride (Si3N4) top layer includes a silicon nitride (Si3N4) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

72. (Previously Added) The circuit of claim 67, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

73. (Previously Added) A circuit on a single substrate, comprising:

a logic device, wherein the logic device includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride (Si3N4) top layer of approximately a third of the first thickness which exhibits a high resistance to oxidation at high temperatures; and

a memory device coupled to the logic device, wherein the memory device further includes a transistor with a second dielectric layer having a second thickness of less than 12 nanometers (nm).

74. (Previously Added) The structure of claim 73, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

75. (Previously Added) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

76. (Previously Added) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO2).

77. (Previously Added) A circuit on a single substrate formed by the method comprising:

forming a logic device including a first transistor and a memory device including a second transistor on a single substrate;

forming a pair of gate oxides on the first transistor and the second transistor to a first thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits resistance to oxidation at high temperatures; and

forming the other of the pair of gate oxides to a second thickness.